DEVELOPING STATIC MODEL OF FAULT CURRENT LIMITER TECHNOLOGIES

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ABSTRACT

Fault Current Limiter (FCL) devices usually have a non-linear and complex transient behaviour during a fault. Standard desktop short-circuit studies carried out by network operators is static analysis (rather than dynamic analysis) which includes calculations of fault levels at peak Making time and Breaking time. In this paper, a methodology for including FCLs in standard short-circuit studies is proposed. The impedance of FCLs obtained from the manufacturers is presented and used to develop computer models for two Resistive Superconducting and Pre-Saturated Core FCLs. This paper is based on learning to date from Western Power Distribution's (WPD) Tier-2 Low Carbon Networks (LCN) Fund project, FlexDGrid.

INTRODUCTION

The UK's renewable energy target which aims to significantly reduce carbon emissions has triggered the increased installation of distributed generators (DGs) e.g. renewables and Combined Heat and Power (CHP) plant in urban distribution networks. An increase in the connection of DGs results in higher system fault levels and consequently network equipment may need to be upgraded for higher short-circuit ratings. One solution to maintain the system fault level within the existing equipment ratings is the deployment of FCL technologies. FCLs can be an economical option compared to conventional network reinforcement, such as transformer or switchgear replacement, which can be prohibitively expensive with long lead times.

FCLs usually have a non-linear and complex transient behaviour during a fault. Constructing a desktop transient model to study their impact on the network's fault levels may be challenging as:

- Detailed parameters of the device may not be provided by the manufacturers due to confidentiality issues;
- Transient models cannot be constructed using conventional power system analysis tools; and
- High technical knowledge for transient modelling and analysis of the device is required.

Moreover, network operators conventionally consider static short-circuit analysis as part of their network planning and connection studies. This includes calculations of fault currents at two post-fault times: i) First peak (Make) and ii) Fault clearance (Break). A fit-for-purpose computer model for FCLs may only include their behaviour at specific snapshots of the fault period e.g. Making and Breaking fault times.

The application of FCLs and developing the steady state desktop model of them was in the scope of FlexDGrid, a LCN Fund project in the UK. In this paper, the methodology developed in FlexDGrid for developing a static desktop model for the FCLs and its inclusion in short-circuit studies is presented.

OVERVIEW OF FLEXDGRID

The central business district of Birmingham, UK, has been identified as an area where a high level of integration of CHP plant is expected in HV (11kV) distribution networks by 2026. As a result of the anticipated level of CHP integration, the fault levels in HV networks could exceed the short-circuit ratings of the switchgear.

FlexDGrid explores the solutions to resolve fault level issues on Birmingham's 11kV network through the trial of three complementary methods:

- *Method Alpha – Enhanced Fault Level Assessment* – Enhancing computer simulation processes to calculate and predict short-circuit currents more accurately.
- *Method Beta – Real-time Management of Fault Level* – Monitoring the electricity network in a greater level of detail than previously possible.
- *Method Gamma – Fault Level Mitigation Technologies* – Installing new technologies that can limit the flow of short-circuit currents when faults occur on the electricity network.

The development of computer static models of FCL technologies trialled in FlexDGrid has been carried out as part of the scope of work in Method Alpha.

OVERVIEW OF TRIALLED FCL

Technologies

Two different FCL technologies were trialled in three primary substations (132/11kV): i) Pre-Saturated Core Fault Current Limiter (PSCFCL) ii) Resistive Superconductive Fault Current Limiter (RSFCL). The RSFCLs were installed in the 11kV network within the busbar coupler of the two primary substations and the PSCFCL in the transformer incomer, as shown in Figure 1(a) and 1(b), respectively. The designed fault current reductions and further details of each trialled FCL are given in Table 1.

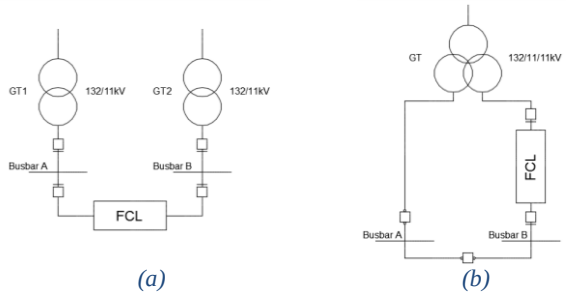


Figure 1: FCLs were inserted in the interconnector between two primary transformers

Table 1: FCL Technologies trialled in FlexDGrid

Primary Substation	Technology	Prospective Break Fault Current	Target Break Fault Current	Break Fault Current Reduction
Castle Bromwich	PSCFCL	6.9	3.7	46%
Chester Street	RSFCL	7.2	3.7	49%
Bournville	RSFCL	8.0	3.0	62%

Resistive Superconducting Fault Current Limiter

An RSFCL is a self-triggered device using high temperature superconductor (HTS) materials. The resistance of the superconductor is very low (almost zero) when its temperature is below a certain level, called critical temperature. However, the resistance significantly increases when the superconductor temperature exceeds the critical temperature.

For an RSFCL application, the HTS is kept to a temperature of approximately 77K using liquid nitrogen [1]. In normal operating conditions, therefore, the impedance of the RSFCL is very low and almost "invisible" to the rest of the network. Under fault conditions, if the current flowing through the RSFCL device exceeds a critical current (Ic), the HTS temperature passes its critical level and therefore the superconductor changes into a conductor with extremely high electrical resistance. Figure 2 compares the resistance characteristics of an RSFCL and a normal conductor [2].

Pre-Saturated Core Fault Current Limiter

A PSCFCL operates with a similar principle to that of a transformer. It consists of two coils windings around a common iron core: i) AC coil (primary winding) connected in series with the network and ii) DC coil (secondary winding) connected to an auxiliary DC source. The iron core forms a path for the magnetic flux induced by the currents flowing through the AC and the DC coils, see Figure 3.

Under normal operating conditions, the iron core is kept saturated by adjusting the DC winding current according to the normal network load (current) passing through the AC winding of the PSCFCL [3]. When the PSCFCL core is saturated, the core's permeability is low, results in proportionally low inductive impedance seen from the AC windings (primary side).

During fault conditions, a high fault current passes through the AC winding which increases AC flux and the core can no longer remain saturated by the DC contribution meaning the core is brought out of saturation. In this condition, the PSCFCL behaves like a high series reactance in the network [3].

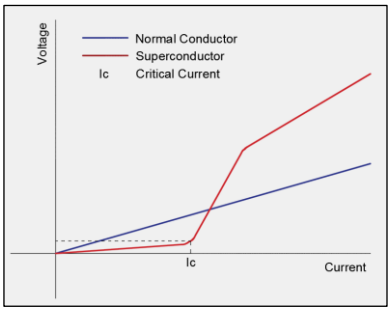


Figure 2: Resistive Superconducting Fault Current Limiter operation diagram

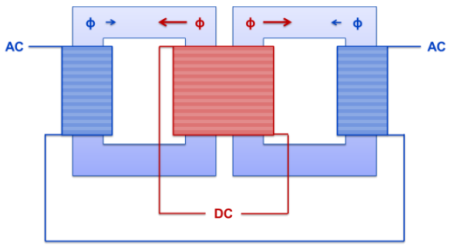


Figure 3: PSCFCL AC and DC windings and their flux directions – in pre-fault operation DC flux is larger than AC flux.

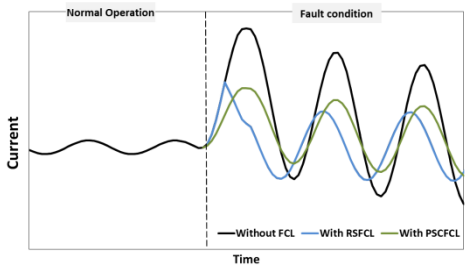


Figure 4: The impact of different FCLs on fault current

Figure 4 shows the impact of the two aforementioned FCLs on the fault current.

METHODOLOGY FOR MODELLING FCL

The impedance of each FCL changes during a fault as a result of changes in the instantaneous and RMS values of the fault current. In other words, FCLs behave similarly to a network branch with large varying impedance during the fault. For the purpose of static short-circuit analysis at a given time (e.g. peak fault time or breaking fault time), the corresponding impedance of an FCL needs to be included in the short-circuit calculations. In order to develop a static model for FCLs trialled in FlexDGrid, a two-stage process was deployed:

- **Stage I –** Obtain device specific impedance data and create impedance look-up tables for prospective Make and Break fault currents. Prospective fault current is the fault current before insertion of the FCL device in the network.
- **Stage II –** Deploy the FCL impedance look-up table in static short-circuit calculations.

Stage I – Create FCL impedance look-up table

FCL manufacturers usually own complex transient computer models of their devices for their detailed design analysis. The level of complexity of these models is not necessary for the conventional static short-circuit calculations carried out by network operators. In addition, due to confidentiality issues, the transient models cannot usually be shared with customers. Nonetheless, these complex models can be used to create a look-up table containing FCL impedances for different prospective fault currents.

In order to model the performance of the three FCLs trialled as part of FlexDGrid, FCL manufacturers were requested to provide the impedance of their devices at pre-fault and post-fault conditions for different network scenarios. This data was used to create the FCL's impedance look-up tables that are inputs to the FCL's static models.

The conventional fault level studies carried out by network operators include the calculation of first instantaneous peak fault level (Making fault level) and RMS of fault level at breaking time (Breaking fault level). Therefore, for each FCL, two impedance look-up tables corresponding to Making and Breaking fault level calculations were constructed.
Section "FCL Impedance Data" presents the detailed procedure of FCL impedance data obtained for different fault currents at Making and Breaking times.

Stage II - Deploy the FCL impedance in static short-circuit analysis

The conventional short-circuit calculation process was modified to include the FCL impact on the calculated fault levels. The proposed process for modelling an FCL impact in short-circuit calculation is as follows:

- Model the FCL as a branch in the case study. The impedance of this branch is the pre-fault impedance of the FCL;
- Run short-circuit analysis to calculate the prospective fault currents (Make and Break) passing through the FCL branch;
- Determine the impedance of the FCL at Make and Break times using the prospective Make and Break fault currents together with the FCL impedance look-up table;
- Create two separate desktop case studies, one for Make and one for Break fault level calculations, where in each case the impedance of the FCL branch is updated accordingly; and
- Run short-circuit analysis to determine Make and Break fault levels with the FCL inserted in the network.

A summary of the methodology for the static modelling of the FCLs is shown in Figure 5.

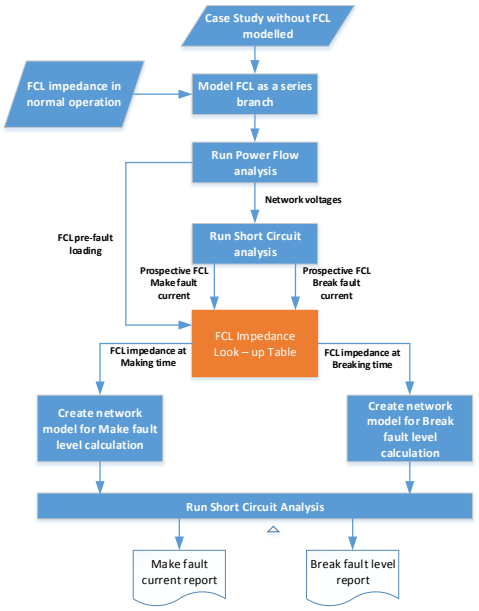


Figure 5: FCL Static Modelling Methodology for Short-circuit Calculation

This proposed methodology can be deployed in any short-circuit studies using power system analysis software e.g. DIgSILENT, Cyme, PSS/E.

FCL IMPEDANCE DATA

Process for obtaining the data

The data for the FCLs was obtained from manufacturers throughout the project. This data was used to create a

look-up table for the static short-circuit analysis where the FCL needs to be considered. The following steps were used to obtain the data:

1. Undertook initial supplier engagement to understand the limitations and extent of their in-house developed model;
2. Provided suppliers with the specific data requirement document describing the network conditions for which the FCL impedance should be calculated;
3. Validated the acquired data for limited cases through laboratory tests. Manufacturers refined their transient models to correct the mismatches identified during the laboratory test; and
4. Carried out data analysis on the FCL impedance data to create a fit-for-purpose look-up table for short-circuit analysis.

One of the main challenges identified through this process was the issue raised by manufacturers that they cannot run their FCL transient models for a large number of network scenarios. This is due to the complexity of the model which requires heavy computation to calculate the FCL impedance for each network condition. Ideally, the FCL impedance needs to be calculated for various combinations of peak making fault current and RMS breaking fault current. However, due to computational limitations, which are different for each FCL and manufacturer, the FCL impedance was calculated for more probable network scenarios. A linear interpolation technique was then used to fill the gaps in data.

PSCFCL Impedance Data

A PSCFCL performs like a large series reactance during a fault. As reported by the manufacturer, the resistance is almost constant around 0.01 Ohm in post-fault network conditions. The reactance of the PSCFCL during the fault depends on the magnitude of the instantaneous current passing through the AC winding; hence the reactance of PSCFCL at a time is independent from the fault current magnitude at other times during the fault. For this reason, two separate PSCFCL look-up tables – one for Make time and one for Break time – must be considered.

The manufacturer was requested to provide the PSCFCL's impedance at fault making time (10ms) and fault breaking time (70ms) for different network scenarios. These network scenarios include different PSCFCL pre-fault loading and different prospective fault currents. The pre-fault loading condition is an important parameter to consider because depending on pre-fault loading, the DC current and consequently DC flux are adjusted to ensure the device core remains saturated during pre-fault (normal load) operation.

The PSCFCL impedance data obtained from the manufacturer is shown in Figure 6 and Figure 7 for Make and Break prospective fault currents, respectively. This data was used to create a look-up table for the PSCFCL impedance. Inputs and outputs of the look-up table for the PSCFCL are shown in Figure 8.

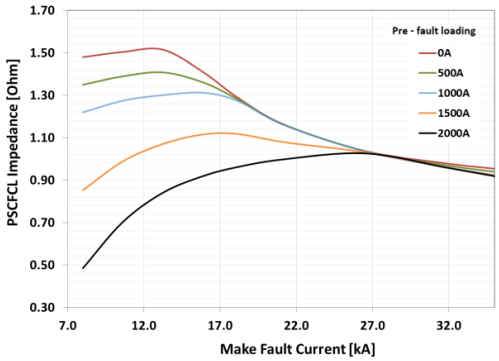


Figure 6 PSCFCL - Impedance (Z) against pre-fault Load Current and Make Short-circuit Current

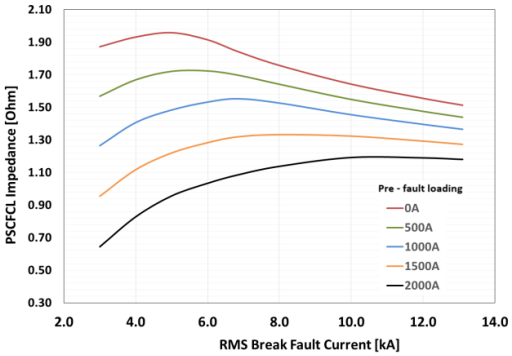


Figure 7 PSCFCL - Impedance (Z) against pre-fault Load Current and Break Short-circuit Current

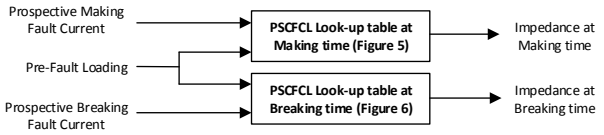


Figure 8: Inputs and outputs to look-up tables for PSCFCL impedance

RSFCL Impedance Data

An RSFCL inserts a high resistance in the network during the fault when the temperature of the superconductor exceeds a critical value. The temperature of the RSFCL device is kept under the critical temperature during the normal conditions using liquid nitrogen and the device operates like a zero impedance branch. The impedance of the RSFCL device during fault, unlike the PSCFCL, is almost independent from the RSFCL's pre-fault loading condition.

The resistance of the RSFCL at a time during a fault may depend on the magnitude of fault currents in previous intervals during the fault. This is due to the amount of heat generated in the HTS during the fault in different intervals. For example, the device's instantaneous

impedance at the breaking time may depend on both Make fault current and Break fault current. This suggests that, for different network conditions (e.g. Networks with different X/R ratio), the RSFCL impedance may be different for the same Breaking fault current.

The manufacturer was requested to provide the impedance of the device for a range of network conditions which result in different Peak (10ms) fault currents and RMS Breaking fault currents at 70ms and 90ms. Figure 9 shows the instantaneous impedance of the RSFCL against corresponding Peak and RMS Breaking fault currents. Looking at data presented in Figure 9, the following points can be noticed:

- Comparing the 10ms, 70ms and 90ms graphs, it appears that the impedance of the RSFCL is incremental during the fault. This is in spite of the fact that fault current is decremented during a fault.

- Fluctuations in the 70ms and 90ms graphs show that the impedance of the RSFCL around the same Breaking fault current may be different. As explained before, this is due to the magnitude of fault currents and the total heat generated in the HTS in previous intervals during the fault (< 70ms).

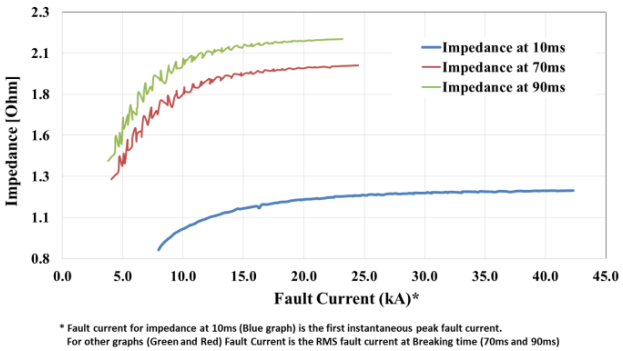
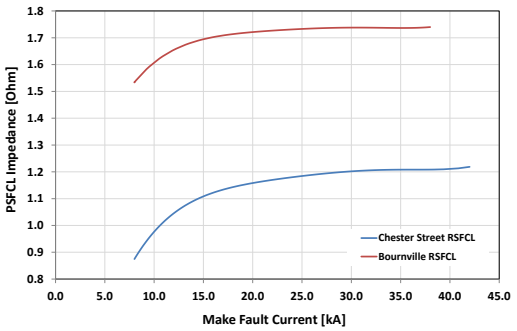
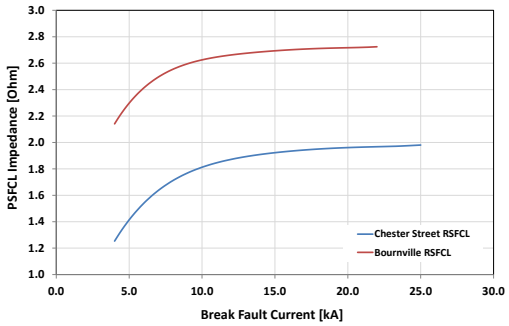


Figure 9: The impedance of the RSFCL at different time during fault considering a wide range of network scenarios

For the purposes of creating a look-up table representing RSFCL impedance against Breaking fault current (independent from fault current at other intervals), the average of the original data obtained from the manufacturer was considered to eliminate the fluctuations shown in Figure 9. The final RSFCL impedance data for the two different RSFCLs trialled in FlexDGrid at Chester Street and Bournville is shown in Figure 10. The impedance of RSFCL during a fault at Bournville is higher than the one in Chester Street because the fault current reduction in Bournville is designed to be higher.



(a)



(b)

Figure 10: Impedance of the two RSFCLs trialled in FlexDGrid (a) against Peak Make current (b) against RMS Break current

CONCLUSIONS

A methodology to include a fit-for-purpose FCL model in conventional static desktop short-circuit analysis was proposed in this paper. The fault current vs impedance characteristics of two FCL technologies, PSCFCL and RSFCL, trialled in FlexDGrid were presented and discussed. Based on the data acquired from the manufacturer it was concluded that two separate impedance look-up tables representing the impedance of the FCL at Make time and Break time can be considered for short-circuit analysis. The proposed methodology and FCL data provided can be used by planning engineers to incorporate in their primary power system analysis software and standard static short-circuit analysis.

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[3] D. Hardman, N. Murdoch and A. Kazerooni, 2016, "SDRC-9 – Installation and Closed-Loop Tests of FLMs and FCLs", *Ofgem SDRC*, Western Power Distribution, UK.